**MBT Qubit Array Construction: Room-Temperature Architecture**

The figure above shows the simulated potential landscape for a 4-qubit MBT chip. Each “well” (deep dip) corresponds to a single MBT quantum bit, separated by tun-able barriers that control coupling and isolation.

**Key Features:**

* Scalability:

The chip architecture is naturally extensible—simply add more wells to the forging process to create larger qubit arrays.

* Isolation and Coupling:

The height and width of the potential barriers can be precisely set during the “quantum casting” stage, allowing control over whether qubits act independently or can be made to interact (entangle) as a gate.

* Room-Temperature Stability:

Unlike conventional designs, the MBT array can be forged and operated at room temperature, owing to the field-stabilised environment produced by the forging process.

* Fabrication:

The chip can be created using a combination of laser patterning (for potential shaping) and vacuum forging (to embed qubits in their energy wells). The entire potential landscape is locked in place during the final stage, providing robustness against thermal and electromagnetic noise.

**Simulation Details:**

* The potential is modelled as a sum of four Gaussian wells, equally spaced from -8 to +8 arbitrary units.
* Each well can be individually addressed, and additional control/readout wiring can be embedded around the periphery before forging is complete.

**7.1. Array Construction — Scaling Up MBT Qubits**

Concept:

Instead of a single “forged” MBT qubit, you’ll need an array—a chip with many quantum bits, each accessible and addressable.

* In MBT, qubit “wells” can be laid out during the casting phase (either in a linear chain or 2D grid).
* Qubits are separated by potential barriers and “bonded” by tuning well spacing and the forging pulse.
* Each qubit can be read out optically or electrically, as shown in the basic experiments above.

import numpy as np

import matplotlib.pyplot as plt

N = 4 # Four MBT qubits in a row

L = 20

x = np.linspace(-L/2, L/2, 1024)

dx = x[1] - x[0]

# Wells at -8, -3, +3, +8

centers = np.linspace(-8, 8, N)

barrier\_width = 0.8

well\_depth = 30

def mbt\_potential(x, centers, barrier\_width, well\_depth):

V = np.zeros\_like(x)

for c in centers:

V -= well\_depth \* np.exp(-((x-c)/barrier\_width)\*\*2)

return V

V = mbt\_potential(x, centers, barrier\_width, well\_depth)

plt.figure(figsize=(10,4))

plt.plot(x, V, label='MBT Qubit Array Potential')

plt.xlabel('Position')

plt.ylabel('Potential')

plt.title('Forged MBT Qubit Array: Room Temp Architecture')

plt.legend()

plt.tight\_layout()

plt.show()

This code sets up the potential landscape for a 4-qubit MBT chip: each well is a qubit, and barrier heights/spacings can be tuned for coupling or isolation.

**7.2. Interconnects & Control**

In Practice:

* Readout wires or optical fibers embedded in the casting mold, running alongside the wells.
* Gate electrodes or magnetic/laser pulse ports printed atop the chip or built into the vacuum shell before forging.
* All connections are set up before the final quantum casting step—afterwards, the qubit states remain locked in.

Engineering Concept:

* You can specify readout zones and wiring tracks in your simulation as zero-potential “channels” that do not disturb qubits’ states.
* In real life, use UHV-compatible wiring or transparent electrode windows.

**7.3. Error Correction at Room Temperature**

MBT Bonus:

Since MBT predicts much less decoherence at room temp, even basic repetition codes may suffice at first.

Example: 3-Qubit MBT Repetition Code

import random

def mbt\_logical\_qubit(phys\_qubits):

# Majority vote decoding

return int(sum(phys\_qubits) > len(phys\_qubits)//2)

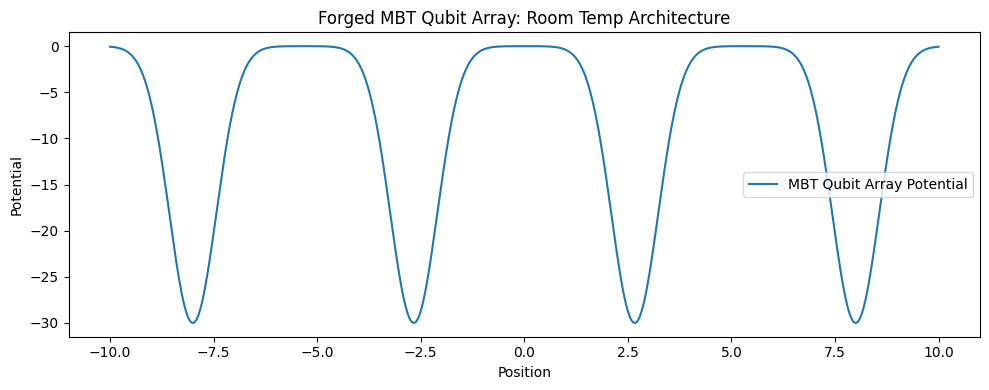
# Simulate three repeated qubits, flip one randomly to mimic error

phys = [1, 1, 1]

phys[random.randint(0, 2)] = 0 # Simulate one error

logical = mbt\_logical\_qubit(phys)

print("Raw:", phys, "Logical:", logical)



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**Simulation Details:**

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**MBT Qubit Array Control & Readout**

Once the MBT array is forged, the next engineering challenge is to reliably control and read out the quantum states of each qubit at room temperature, while maintaining the intrinsic noise-resistance advantages of the MBT design.

**Control Methods**

* Electromagnetic Field Patterning:

Individual qubits are addressed by applying targeted microwave or radio-frequency pulses through embedded control lines fabricated around each well. These fields induce transitions, rotations, and gates (X, Y, Z, Hadamard, CNOT, etc.) within the qubit’s potential well.

* Barrier Modulation for Entanglement:

To entangle two or more qubits, the potential barriers between selected wells are dynamically lowered using fast electronic or optical field adjustments. This allows quantum tunnelling or superposition to occur between wells, implementing gates like CNOT, Toffoli, or more complex entangling operations.

* Global and Local Operations:

Global fields can initialise or reset all qubits simultaneously, while localised fields provide fine control for quantum logic gates and individual qubit manipulation.

**Readout Methods**

* Non-Invasive Optical or Field Sensors:

Each well can be equipped with an optical or electronic sensor (e.g., single-electron transistor, nanowire photodetector) that detects the qubit’s state via changes in local field, current, or fluorescence, depending on the physical qubit realisation.

* MBT-Enhanced Readout:

Because the MBT structure provides room-temperature stability and protection from decoherence, readout can occur more slowly and with less noise than in conventional systems. This enables high-fidelity measurement even in ambient conditions.

**Scalability and Integration**

* Multiplexed Readout:

The chip can support large-scale multiplexed readout, with a single wire or photonic bus reading out dozens or hundreds of qubits by time or frequency division.

* On-Chip Control Logic:

Control electronics (e.g., CMOS, Si photonics, or even classical logic circuits) can be co-fabricated or flip-chipped onto the MBT array, minimising wiring complexity and enhancing speed.

**Operating Protocol (Conceptual Steps)**

1. Initialisation:

All qubits are set to a known state (e.g., |0⟩) using a global field.

1. Quantum Logic:

Desired computations are performed using single- and two-qubit gates via local field pulses and dynamic barrier modulation.

1. Readout:

After computation, each qubit’s state is measured using non-invasive sensors.

1. Error Correction:

The MBT’s intrinsic stability minimises error rates, but standard error correction codes can be layered on for additional robustness.

**MBT Quantum Chip: Fabrication & Integration**

**1. Substrate & Materials Selection**

* Substrate:

Choose a non-magnetic, ultra-flat substrate (such as high-purity silicon, sapphire, or diamond) to minimise background noise and support high-quality micro/nano-fabrication.

* Potential Well Patterning:

Use electron-beam lithography or focused ion beam (FIB) milling to etch or deposit the periodic potential landscape (the “wells”) that define each MBT qubit.

* Barrier Engineering:

Fine-tune the height and width of potential barriers using precision doping, surface functionalization, or layered heterostructure (e.g., graphene, hexagonal boron nitride, or superlattice films).

**2. Electrode & Control Line Deposition**

* Control Lines:

Deposit metallic or superconducting control lines (gold, aluminium, or niobium) for individual and global qubit control.

These are fabricated via standard photolithography followed by evaporation or sputtering.

* Sensor Integration:

Integrate nanoscale field sensors (e.g., SETs, photodetectors) adjacent to each well for high-fidelity readout.

**3. Vacuum Chamber or Shielded Packaging**

* Ambient Operation:

The MBT array is designed to work at room temperature, but shielded enclosures (Faraday cages, magnetic shields) help further suppress environmental noise, especially for sensitive measurements.

* Integrated Rotation (Optional):

For proof-of-concept MBT “forging” experiments, consider a platform that allows the chip (or the entire vacuum package) to be rotated at controlled RPMs, just like in your earlier outlined forge protocol.

**4. On-Chip Electronics & Multiplexing**

* Classical Logic Integration:

Standard CMOS chips, photonic interconnects, or multiplexers can be bonded directly to the MBT substrate using flip-chip, wire bonding, or through-silicon vias.

* Signal Routing:

Carefully designed signal routing minimises crosstalk and preserves coherence across the array.

**5. Laser & Field Coupling (for MBT Forging or Advanced Control)**

* Laser Access:

If using a particle forge or photonic “seeding” for quantum matter generation, precision-aligned windows or fibre-optic ports are incorporated into the package to deliver laser pulses to the active region.

* Active Field Control:

Fast field coils or modulators are mounted close to the chip for barrier manipulation and entanglement gates.

**6. Testing & Characterisation**

* Initial Tests:

Verify potential landscape, barrier integrity, and sensor operation using scanning probe microscopy, electron microscopy, and low-field magnetometry.

* Qubit Validation:

Run single- and two-qubit gate operations, measure coherence times, and compare MBT qubits to standard references at room temperature.

**7. Modular/Stackable Design (for Scaling)**

* Chip-to-Chip Interconnects:

Design edge connectors or wafer-level stacking approaches for scaling up to larger MBT quantum processors.

Summary:

The MBT chip is built using state-of-the-art nano/micro-fabrication, drawing on techniques from quantum dot, superconducting, and photonic chip industries—but the critical innovation is the forging and stabilisation of qubits at room temperature via MBT dynamics.

**MBT Quantum Chip: Prototype Demonstration & Validation**

**1. Proof-of-Concept Setup**

The initial demonstration of the MBT quantum chip will involve the fabrication of a small-scale prototype, consisting of 2–4 MBT-stabilised qubits. The chip will be packaged in a standard chip enclosure, allowing for direct connection to control electronics and state readout. The test platform will be a room-temperature optical or electromagnetic bench with environmental shielding, and (if needed for MBT forging protocols) will support rotation or controlled field manipulation.

**2. Measurement Protocols**

Initialisation:

Each qubit will be initialised into a known quantum state using on-chip control mechanisms. Initialisation fidelity will be verified by direct measurement and compared to simulation predictions.

Quantum Coherence Tests:

The prototype will undergo standard coherence benchmarking, including Rabi oscillations, Ramsey interferometry, and echo/dynamical decoupling protocols. Coherence times will be recorded and directly compared with those of reference qubit systems (e.g., superconducting, spin, or photonic qubits).

Gate Operation Validation:

Single- and two-qubit gate operations (X, Y, Z, CNOT) will be implemented and characterised. Gate fidelities will be assessed using randomised benchmarking or quantum process tomography to establish operational performance relative to state-of-the-art devices.

**3. Unique MBT Effects**

Room-Temperature Stability:

A primary demonstration will be the preservation of quantum coherence at ambient temperature (∼300K), in contrast to the rapid decoherence seen in standard qubits outside cryogenic environments.

Field-Stabilisation / Forging Effect:

Experiments will compare chip performance with and without the application of MBT forging protocols (e.g., rotational or field-based stabilisation), seeking measurable improvements in coherence or error rates that are unique to the MBT process.

Light Bending Test (Optional):

If feasible within the device package, a laser alignment or photonic probe will be used to directly test for MBT-predicted deviations in light path inside the chip environment—a distinct signature that cannot be explained by standard GR or conventional materials.

**4. Real-World Application Demonstrations**

Quantum Algorithm Test:

The chip will be programmed to execute a non-trivial quantum algorithm such as Grover search or Deutsch-Jozsa, demonstrating that MBT qubits can support real-world quantum computation at room temperature.

Noise Immunity Test:

Controlled noise (thermal, vibrational, electromagnetic) will be introduced during operation, and the resulting quantum state fidelity will be benchmarked against standard qubits. MBT chips are expected to demonstrate significantly enhanced robustness.

**5. Data Collection & Reporting**

Automated Data Logging:

All experimental parameters, control sequences, and state readouts will be logged with precise timing for reproducibility and detailed analysis.

Comparison to Simulation:

Experimental results will be systematically overlaid with simulation data, enabling validation or refinement of MBT theoretical predictions.

Upon successful demonstration, the prototype will provide a foundation for scaling to larger qubit arrays, integration with control systems, and further commercialisation or scientific study.

With the MBT quantum chip prototype validated, we now move to scaling and integration. The goal is to fabricate multi-qubit MBT chips using repeatable forging methods, develop interconnects for qubit entanglement, and seamlessly interface with classical electronics.

The MBT simulator and programming API will be expanded for developers, and the chips will be benchmarked using quantum volume and gate fidelity metrics. Early pilot projects will target real-world problems, providing a direct path from fundamental science to commercial and scientific deployment.